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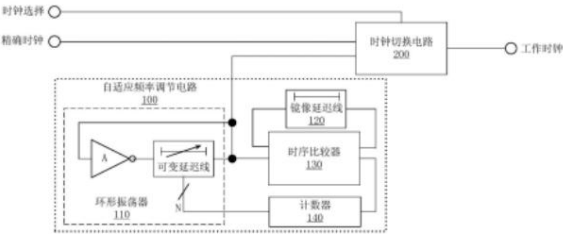
2 pages of claims 6 pages of specification 3 pages of drawings

(54) Invention Name:

Adaptive Frequency Adjustment Method, Circuit and Circuit System

(57) Abstract:

The present invention provides an adaptive frequency adjustment method, circuit and circuit system, wherein the adaptive frequency adjustment circuit comprises: a ring oscillator, which outputs a variable frequency, wherein the ring oscillator comprises: a variable delay line and an inverter whose two ends are respectively connected to the output end and the input end of the variable delay line; a mirror delay line, which mirrors the line with the worst delay in the same power domain in the circuit system; a timing comparator, which is respectively connected to the ring oscillator and the mirror delay line, and is used to compare whether the output timing of the ring oscillator is the same as the output timing of the mirror delay line, and feeds back the comparison result to the ring oscillator, so that the ring oscillator can adjust the frequency until the output timing of the ring oscillator is the same as the output timing of the mirror delay line. The present invention can realize the adaptation of the working frequency, process, voltage and temperature. Through the technical solution of the present invention, the consistency, stability and performance of the chip can be improved.



1. An adaptive frequency adjustment circuit, applied to a circuit system, characterized in that the adaptive frequency adjustment circuit comprises: a ring oscillator, outputting a variable frequency; a mirror delay line, mirroring a line with the worst delay in the same power domain of the circuit system; a timing comparator, connected to the ring oscillator and the mirror delay line, respectively, for comparing whether the output timing of the ring oscillator is the same as the output timing of the mirror delay line, and feeding back the comparison result to the ring oscillator for the ring oscillator to adjust the frequency until the output timing of the ring oscillator is the same as the output timing of the mirror delay line; when the output timing of the ring oscillator is the same as the output timing of the mirror delay line, the ring oscillator is adjusted.

The clock generated by the device is used as the working clock of the circuit system.

2. The adaptive frequency adjustment circuit according to claim 1, characterized in that the ring oscillator comprises: A variable delay line and an inverter with two ends respectively connected to the output end and the input end of the variable delay line.

3. The adaptive frequency adjustment circuit according to claim 2, characterized in that the variable delay line comprises a delay line and a switch for adjusting the length of the delay line. 4. The adaptive frequency adjustment circuit according to claim 2 or 3, characterized in that a counter is connected between the ring oscillator and the timing comparator, for counting the output pulses of the timing comparator when the output timing of the ring oscillator is different from the output timing of the mirror delay line; the ring oscillator changes the length of the variable delay line according to the counting result of the counter.

5. An adaptive frequency adjustment method, characterized in that it comprises: the adaptive frequency adjustment method comprises: outputting a variable frequency through a ring oscillator; mirroring a line with the worst delay in the same power domain in a circuit system through a mirror delay line; comparing the output timing of the ring oscillator and the output timing of the mirror delay line through a timing comparator to see whether they are the same, and feeding back the comparison result to the ring oscillator for the ring oscillator to adjust the frequency until the output timing of the ring oscillator and the output timing of the mirror delay line are the same;

When the output timing of the ring oscillator is the same as the output timing of the mirror delay line, the ring oscillator The clock generated by the device is used as the working clock of the circuit system.

6. The adaptive frequency adjustment method according to claim 5, characterized in that the ring oscillator comprises: A variable delay line and an inverter with two ends respectively connected to the output end and the input end of the variable delay line.

7. The adaptive frequency adjustment method according to claim 6, characterized in that the variable delay line comprises a delay A delay line and a switch for adjusting the length of the delay line.

8. The adaptive frequency adjustment method according to claim 6 or 7 is characterized in that a counter is connected between the ring oscillator and the timing comparator, for counting the output pulses of the timing comparator when the output timing of the ring oscillator and the output timing of the mirror delay line are different; the ring oscillator changes the length of the variable delay line according to the counting result of the counter.

9. A circuit system, characterized in that it comprises the circuit system as claimed in any one of claims 1 to 4 Adaptive frequency adjustment circuit.

10. The circuit system according to claim 9, characterized in that the circuit system comprises an ASIC or a SOC. 11. The circuit system according to claim 9, characterized in that the initial clock of the circuit system adopts a clock generated by a crystal oscillator and output via a phase-locked loop.

12. The circuit system according to claim 9 or 11, characterized in that the circuit system comprises a clock switching circuit, which is used to use the clock generated by the ring oscillator as the working clock of the circuit system when the output timing of the ring oscillator and the output timing of the mirror delay line are the same.

Adaptive frequency adjustment method, circuit and circuit system

Technical Field

[0001] The present invention relates to the field of circuit technology, and in particular to the field of clock circuit technology, and specifically to an adaptive frequency adjustment method, circuit, and circuit system.

Background

[0002] With the improvement of integrated circuit performance and process, problems such as circuit power consumption and process fluctuation have an increasingly greater impact on chip yield, performance consistency and product

stability. [0003] Due to factors in chip process, there are differences between individual chips, and the frequency at which different chips can work stably at the same working voltage will be different. Based on the measured "frequency-voltage" table, it is necessary to cover the individual differences between chips. When performing "frequency-voltage" stability tests on a large number of chips, a long-term stability test is performed on the working voltage corresponding to each working frequency point.

[0004] At the same working frequency, chips with poor performance require a higher working voltage, while chips with good performance require a relatively low working voltage. Therefore, the "frequency-voltage" tested in this way is higher for chips with better performance when taking into account chips with poor performance. As a result, when the voltage of chips with good performance is set according to the "frequency-voltage" table, the working voltage of chips with good performance is higher than the actual performance requirement, and the power consumption will also be correspondingly

higher. [0005] There is an error in the output voltage of the power chip, so in actual use, it is necessary to consider the voltage error output by the power chip and increase the voltage value in the "frequency-voltage" table according to the corresponding proportion. In order to cover the power chip with negative deviation, the power chip with positive deviation will be higher, and the power consumption will be

higher accordingly. [0006] The transient response performance of the power chip is difficult to meet the needs of high-performance chips. When the chip load suddenly increases, the power chip cannot respond. Usually, there will be a few microseconds to more than ten microseconds when the filter capacitor on the power supply needs to provide energy. At this time, the power supply voltage will drop, and this is when the chip needs stable power supply. Therefore, the "frequency-voltage" table will also consider the lowest voltage point during the time when the power supply does not respond, so the voltage value in the table has to be further increased, which leads to a further increase in power consumption.

[0007] AVS is limited by the response speed of the power module. Currently, the response speed of most power supplies is at the microsecond level. For ASIC/SOC operating at a GHz frequency, some logic operations only require a few nanoseconds, and the response speed at the microsecond level is obviously too slow. During the period when the power module is not responding, the voltage may have dropped to a level that causes the circuit to work unstably, resulting in problems such as freezing.

[0008] The measurement of the frequency-voltage table required by the DVS method requires a lot of manpower and a lot of testing work, and the control of performance and power consumption is difficult to optimize. The AVS method can be adaptive in terms of process and temperature, but it is difficult to meet the increasingly high performance requirements in terms of the speed of voltage control. [0009] In summary,

the existing technologies all determine the operating frequency based on performance requirements, and the power supply, process, and temperature are all developed around the determined frequency. The factors of power supply, process, and temperature are all objective existences, which bring many constraints to chip quality control and application. This is the biggest disadvantage of the existing technical solutions.

In view of the

above - mentioned shortcomings of the prior art, the present invention aims to provide an adaptive frequency adjustment method.

A method, a circuit and a circuit system are used to solve the problem that it is difficult to adaptively adjust the frequency in the prior art. [0011] To achieve the above purpose and other related purposes, the present invention provides an adaptive frequency adjustment circuit, which is applied to a circuit system, wherein the adaptive frequency adjustment circuit includes: a ring oscillator, which outputs a variable frequency; a mirror delay line, which mirrors the line with the worst delay in the same power domain in the circuit system; a timing comparator, which is respectively connected to the ring oscillator and the mirror delay line, and is used to compare whether the output timing of the ring oscillator and the output timing of the mirror delay line are the same, and feed back the comparison result to the ring oscillator, so that the ring oscillator can adjust the frequency until the output timing of the ring oscillator and the output timing of the mirror delay line are the same. [0012] In one embodiment of the present invention, when the output timing of the ring oscillator and the output timing of the mirror delay line are the same, the clock generated by the ring oscillator is used as the working clock of the circuit system. [0013] In one embodiment of the present invention, the ring oscillator includes: a variable delay line and an inverter whose two ends are respectively connected to the output end and the input end of the variable delay line. [0014] In one embodiment of the present invention, the variable delay line includes a delay line and a switch for adjusting the length of the delay line. [0015] In one embodiment of the present invention, a counter is connected between the ring oscillator and the timing comparator, for counting the output pulses of the timing comparator when the output timing of the ring oscillator and the output timing of the mirror delay line are different; the ring oscillator changes the length of the variable delay line according to the counting result of the counter. [0016] An embodiment of the present invention also provides an adaptive frequency adjustment method, comprising: the adaptive frequency adjustment method comprises: outputting a variable frequency through a ring oscillator; mirroring the line with the worst delay in the same power domain in the circuit system through a mirror delay line; comparing the output timing of the ring oscillator and the output timing of the mirror delay line through a timing comparator to see if they are the same, and feeding back the comparison result to the ring oscillator for the ring oscillator to adjust the frequency until the output timing of the ring oscillator and the output timing of the mirror delay line are the same. [0017] In one embodiment of the present invention, when the output timing of the ring oscillator and the output timing of the mirror delay line are the same, the clock generated by the ring oscillator is used as the working clock of the circuit system. [0018] In one embodiment of the present invention, the ring oscillator includes: a variable delay line and an inverter whose two ends are respectively connected to the output end and the input end of the variable delay line. [0019] In one embodiment of the present invention, the variable delay line includes a delay line and a switch for adjusting the length of the delay line. [0020] In one embodiment of the present invention, a counter is connected between the ring oscillator and the timing comparator, which is used to count the output pulses of the timing comparator when the output timing of the ring oscillator and the output timing of the mirror delay line are not the same; the ring oscillator changes the length of the variable delay line according to the counting result of the counter. [0021] An embodiment of the present invention also provides a circuit system, including the adaptive frequency adjustment circuit as described above. [0022] In one embodiment of the present invention, the circuit system includes an ASIC or a SOC. [0023] In one embodiment of the present invention, the initial clock of the circuit system adopts a clock generated by a crystal oscillator and output via a phase-locked loop. [0024] In one embodiment of the present invention, the circuit system includes a clock switching circuit, which is used to use the clock generated by the ring oscillator as the working clock of the circuit system when the output timing of the ring oscillator and the output timing of the mirror delay line are the same.

[0025] As described above, the adaptive frequency adjustment method, circuit and circuit system of the present invention have the following beneficial effects:

[0026] The present invention can realize the adaptation of working frequency, process, voltage and temperature. Through the technical solution of the present invention, the consistency, stability and performance of the chip can be improved.

BRIEF

DESCRIPTION OF THE DRAWINGS [0027] FIG. 1 is a schematic diagram of a frequency adjustment

process in the prior art. [0028] FIG. 2 is a schematic diagram of a frequency adjustment process of an adaptive frequency adjustment method

of the present invention. [0029] FIG. 3 is a schematic diagram of a process of an adaptive frequency adjustment method of the present invention

in an embodiment. [0030] FIG. 4 is a schematic diagram of a principle of an adaptive frequency adjustment circuit of the present invention in an

embodiment. [0031] DESCRIPTION OF

COMPONENT NUMBERS [0032] 100 Adaptive frequency adjustment circuit

[0033] 110 Ring oscillator Mirror

[0034] 120 delay line Timing

[0035] 130 comparator Counter

[0036] 140 Clock

[0037] 200 switching circuit

Steps S110 to S130

Specific implementation

[0039] The following describes the implementation of the present invention through specific examples. Those skilled in the art can easily understand other advantages and effects of the present invention from the content disclosed in this specification. The present invention can also be implemented or applied through other different specific implementations. The details in this specification can also be modified or changed based on different viewpoints and applications without departing from the spirit of the present invention. It should be noted that the following embodiments and the features in the embodiments can be combined with each other without conflict.

[0040] Please refer to Figures 1 to 4. It should be

noted that the illustrations provided in the following embodiments are only schematic illustrations of the basic concept of the present invention. Therefore, the diagrams only show the components related to the present invention rather than the number, shape and size of the components in the actual implementation. The type, quantity and proportion of each component in the actual implementation can be changed at will, and the component layout type may also be more complicated. [0041] The process of frequency adjustment in the prior art is shown

in Figure 1. After the ASIC/SOC is powered on, the operating voltage corresponding to the target frequency is found from the frequency voltage table. The formulation of the frequency voltage table requires testing and screening of a large number of chips, and the deviations in the process and voltage of the entire batch of chips to be tested must be taken into account. Then set the target voltage, delay, wait for the power supply to stabilize, and finally make the actual frequency = the set value. [0042] The purpose of this

embodiment is to provide an adaptive frequency adjustment method, circuit and circuit system to solve the problem that it is difficult to adaptively adjust the frequency in the prior art. [0043] The principle flow of the adaptive frequency adjustment method, circuit and circuit system provided by this embodiment is shown in Figure 2.

After the ASIC/SOC is powered on, the critical path delay is tested. Each chip can obtain its own corresponding delay data, which is independent of other chips. The frequency of the ring oscillator is adjusted according to the test results, and the working clock is switched to the ring oscillator. The adaptive frequency adjustment is completed.

[0044] The adaptive frequency adjustment method, circuit and circuit system provided in this embodiment make the working frequency change with the change of voltage, process and temperature, realize adaptive frequency adjustment, and make the working clock frequency of ASIC/SOC automatically adjust to the frequency suitable for process, voltage and temperature. The reading of the actual working frequency can use an accurate crystal clock to generate an accurate time gate as the counting time of the working clock, and the average frequency of the actual working clock is obtained by calculation. [0045] The principle and implementation method of the adaptive frequency adjustment method, circuit and circuit system of the present invention will be described in detail below, so that those skilled in the art can understand the adaptive frequency adjustment method, circuit and circuit system of the present invention without creative work. [0046] Specifically, as shown in FIG3, the present invention provides an adaptive frequency adjustment method, and the adaptive frequency adjustment method includes the following steps: [0047] Step S110, outputting a variable frequency through a ring oscillator. [0048] Specifically, in this embodiment, the ring oscillator includes: a variable delay line and an inverter whose two ends are respectively connected to the output end and the input end of the variable delay line. [0049] Wherein, the variable delay line includes a delay line and a switch for adjusting the length of the delay line. [0050] That is, the variable delay line can change its length through a switch, thereby changing the delay time, and loop back to the input of the delay line through an inverter to form a variable frequency ring oscillator. [0051] Step S120, mirror the line with the worst delay in the same power domain of the circuit system through a mirror delay line. That is, the mirror delay line is a copy of the worst delay path in the ASIC/SOC in the same power domain. Because the mirror delay line is a copy of the worst delay path in the ASIC/SOC, the mirror delay line can characterize the impact of voltage, process, and temperature on the worst delay path in the circuit system (ASIC/SOC) to the greatest extent. [0052] Step S130, compare the output timing of the ring oscillator and the output timing of the mirror delay line through a timing comparator to see if they are the same, and feed back the comparison result to the ring oscillator so that the ring oscillator can adjust the frequency until the output timing of the ring oscillator is the same as the output timing of the mirror delay line. [0053] The output of the ring oscillator is used as a driving clock for a timing comparator, and the timing comparator is used to compare the timing output results of the mirror delay line and the timing output results of the mirror delay line. If the comparison results are consistent, it means that the delay of the mirror delay line will not cause a timing logic error, and the worst delay path in the corresponding ASIC/SOC meets the timing requirements; otherwise, it means that the worst delay in the ASIC/SOC will cause a timing logic error and output an error pulse at the falling edge of the current clock. [0054] In this embodiment, when the output timing of the ring oscillator and the output timing of the mirror delay line are the same, the clock generated by the ring oscillator is used as the working clock of the circuit system. [0055] In this embodiment, a counter is connected between the ring oscillator and the timing comparator, which is used to count the output pulses of the timing comparator when the output timing of the ring oscillator and the output timing of the mirror delay line are different; the ring oscillator changes the length of the variable delay line according to the counting result of the counter. [0056] The counter adds and counts the error pulses of the timing comparator, and uses the counting result to change the length of the variable delay line. The increase in the count value corresponds to the increase in the length of the delay line, thereby reducing the frequency of the ring oscillator. This is a closed-loop feedback process. Only when the frequency of the ring oscillator is reduced to a level consistent with the comparison result in the timing comparator, the timing comparator will stop generating error pulses, the counter will stop counting, and the length of the delay line will be determined. [0057] An embodiment of the present invention also provides an adaptive frequency adjustment circuit 100, which is applied to a circuit system. As shown in FIG4, the adaptive frequency adjustment circuit 100 includes: a ring oscillator 110, a mirror delay line 120, a timing comparator 130 and a counter 140.

[0058] The adaptive frequency adjustment circuit 100 in this embodiment is described in detail below. [0059] In this embodiment, the ring oscillator 110 outputs a variable frequency. [0060] Specifically, in this embodiment, the ring oscillator 110 includes: a variable delay line and an inverter whose two ends are respectively connected to the output end and the input end of the variable delay line. The variable delay line includes a delay line and a switch for adjusting the length of the delay line. That is, the variable delay line can change its length through the switch, thereby changing the delay time, and loop back to the input of the delay line through an inverter to form a variable frequency ring oscillator 110. [0062] In this embodiment, the mirror delay line 120 mirrors the line with the worst delay in the same power domain in the circuit system (ASIC/SOC); that is, the mirror delay line 120 is a copy of the worst delay path in the ASIC/SOC in the same power domain. Because the mirror delay line 120 is a replica of the worst delay path in the ASIC/SOC, the mirror delay line 120 can characterize the influence of voltage, process, and temperature on the worst delay path in the circuit system (ASIC/SOC) to the greatest extent. [0063] In this embodiment, the timing comparator 130 is connected to the ring oscillator 110 and the mirror delay line 120 respectively, and is used to compare whether the output timing of the ring oscillator 110 is the same as the output timing of the mirror delay line 120, and feed back the comparison result to the ring oscillator 110, so that the ring oscillator 110 can adjust the frequency until the output timing of the ring oscillator 110 is the same as the output timing of the mirror delay line 120. [0064] The output of the ring oscillator 110 is used as a driving clock of the timing comparator 130, and the timing comparator 130 is used to compare the timing output results of the mirror delay line 120 and the timing output results of the mirror delay line 120. If the comparison results are consistent, it means that the delay of the mirror delay line 120 will not cause a timing logic error, and the worst delay path in the corresponding ASIC/SOC meets the timing requirements; otherwise, it means that the worst delay in the ASIC/SOC will cause a timing logic error and output an error pulse at the falling edge of the current clock. [0065] In this embodiment, when the output timing of the ring oscillator 110 is the same as the output timing of the mirror delay line 120, the clock generated by the ring oscillator 110 is used as the working clock of the circuit system. [0066] In this embodiment, the counter 140 is connected between the ring oscillator 110 and the timing comparator 130, and is used to count the output pulses of the timing comparator 130 when the output timing of the ring oscillator 110 is different from the output timing of the mirror delay line 120; the ring oscillator 110 changes the length of the variable delay line according to the counting result of the counter 140. [0067] The counter 140 counts the error pulses of the timing comparator 130, and uses the counting result to change the length of the variable delay line. The increase in the count value corresponds to the increase in the length of the delay line, thereby reducing the frequency of the ring oscillator 110. This is a closed-loop feedback process. Only when the frequency of the ring oscillator 110 is reduced to the same level as the comparison result in the timing comparator 130, the timing comparator 130 will stop generating error pulses, the counter 140 will stop counting, and the length of the delay line will be determined. [0068] After the timing comparator 130 no longer generates error pulses, the working clock of the circuit system (ASIC/SOC) can be switched to the clock generated by the adaptive clock circuit. Because the mirror delay line 120 is a replica of the worst delay path in the ASIC/SOC, the mirror delay line 120 can characterize the impact of voltage, process, and temperature on the worst delay path in the ASIC/SOC to the greatest extent. Due to the closed-loop feedback process described above, the clock frequency generated by the ring oscillator 110 where the variable delay line is located has made the mirror delay line 120 no longer produce timing errors, so the clock generated by the adaptive clock circuit can also meet the timing requirements of the worst delay path in the ASIC/SOC. Since the adaptive frequency adjustment circuit 100 and the ASIC/SOC are in the same power domain and adjacent to each other on the chip, the differences in voltage, process, and temperature are very small.

Therefore, when the voltage, process and temperature of the ASIC/SOC change, the clock frequency generated by the adaptive clock circuit will also change accordingly, and the timing constraints of the mirror delay line 120 can always be met, so that the timing comparator 130 does not generate a timing error pulse, that is, the worst delay path in the ASIC/SOC does not have a timing error. [0069] In the

case where the response speed of the power module and the PLL (Phase Locked Loop) is not enough to meet the performance requirements of the circuit system, the adaptive frequency adjustment circuit 100 of this embodiment automatically and quickly adjusts the operating frequency to adapt to the changes in the power supply voltage, chip process and chip temperature, which can greatly reduce the difficulty of product testing and application, and also improve the consistency of

the product. [0070] The adaptive frequency adjustment circuit 100 of this embodiment has the above-mentioned essential differences from the technical solutions of the prior art, and at the same time has all the advantages of the above-mentioned technical solutions. The adaptive frequency adjustment in the adaptive frequency adjustment circuit 100 of this embodiment is completely automatically implemented, and does not require software to be involved in the setting, so the adjustment speed is the fastest, and can well follow the voltage changes and achieve a single clock level

response speed, that is, a nanosecond or even picosecond level response time. [0071] An embodiment of the present invention further provides a circuit system, comprising the adaptive frequency adjustment circuit 100 as described above. [0072] In

this embodiment, the circuit system includes but is not limited to an ASIC or a SOC. [0073] In this embodiment, the initial clock of the circuit system

adopts a clock generated by a crystal oscillator and output via a phase-locked loop. [0074] In this embodiment, the circuit system includes a clock switching circuit 200, which is used to use the clock generated by the ring oscillator 110 as the working clock of the circuit system when the output timing of the ring oscillator 110 and the output timing of

the mirror delay line 120 are the same. [0075] In the initial state of the circuit system, the working clock is selected by the clock switching circuit 200 as a precise clock. The precise clock is a clock generated by a crystal oscillator and output via a PLL (phase-locked loop), which has higher clock accuracy and stability, which Initial clock of ASIC/SOC.

[0076] The chip in the ASIC/SOC only needs to switch the working clock to the "precise clock" by default after power-on reset, and start the adaptive frequency adjustment circuit 100. After the timing comparator 130 in the adaptive frequency adjustment circuit 100 no longer generates counting pulses, the working clock is switched to the clock generated in the adaptive frequency adjustment circuit 100, so that the setting of the adaptive frequency adjustment is completed. Since the adaptive frequency adjustment circuit 100 and the ASIC/SOC are in the same power domain and adjacent to each other on the chip, the differences in voltage, process, and temperature are very small. Therefore, when the voltage, process, and temperature of the ASIC/SOC change, the clock frequency generated by the adaptive clock circuit will also change accordingly, and the timing constraints of the mirror delay line 120 can always be met, so that the timing comparator 130 does not generate a timing error pulse, that is, the worst delay path in the ASIC/SOC does not have a timing error. [0077] In

summary, the present invention can realize the adaptation of the working frequency, process, voltage, and temperature. Through the technical solution of the present invention, the consistency, stability, and performance of the chip can be improved. Therefore, the present invention effectively overcomes various shortcomings in the prior art and has a high

industrial utilization value. [0078] The above embodiments are only illustrative of the principles and effects of the present invention, and are not intended to limit the present invention. Anyone familiar with the technology can modify or change the above embodiments without violating the spirit and scope of the present invention. Therefore, all equivalent modifications or changes made by those with ordinary knowledge in the technical field without departing from the spirit and technical ideas disclosed by the present invention should still be covered by the claims of the present invention.

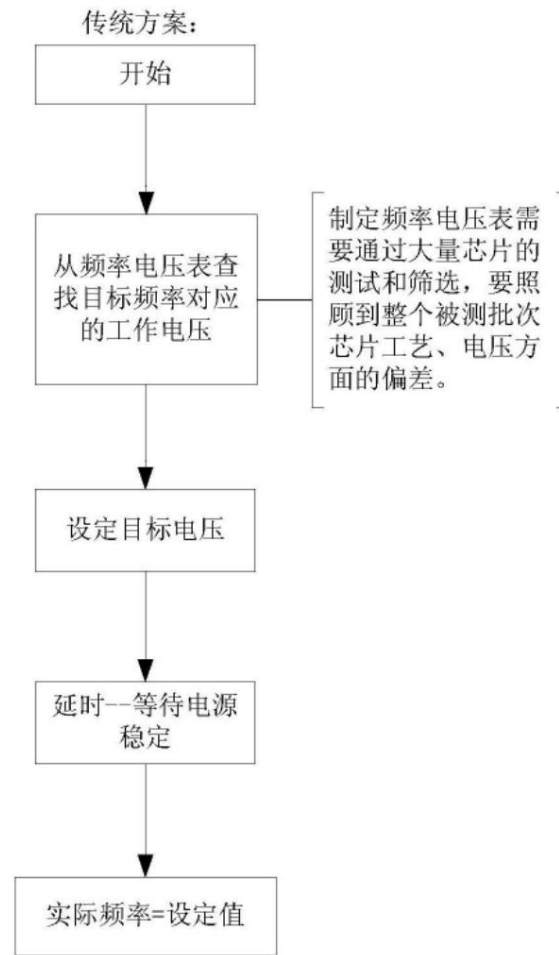


Figure 1

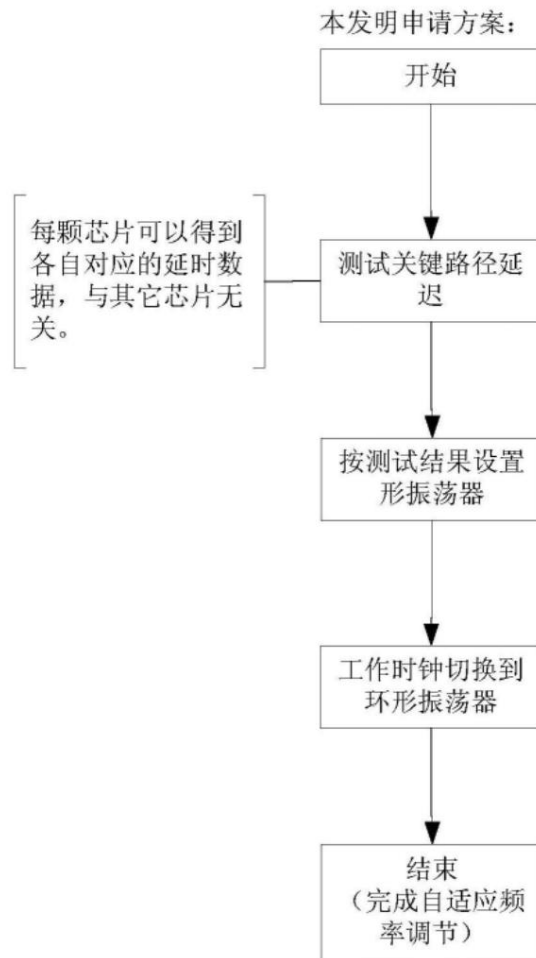


Figure 2

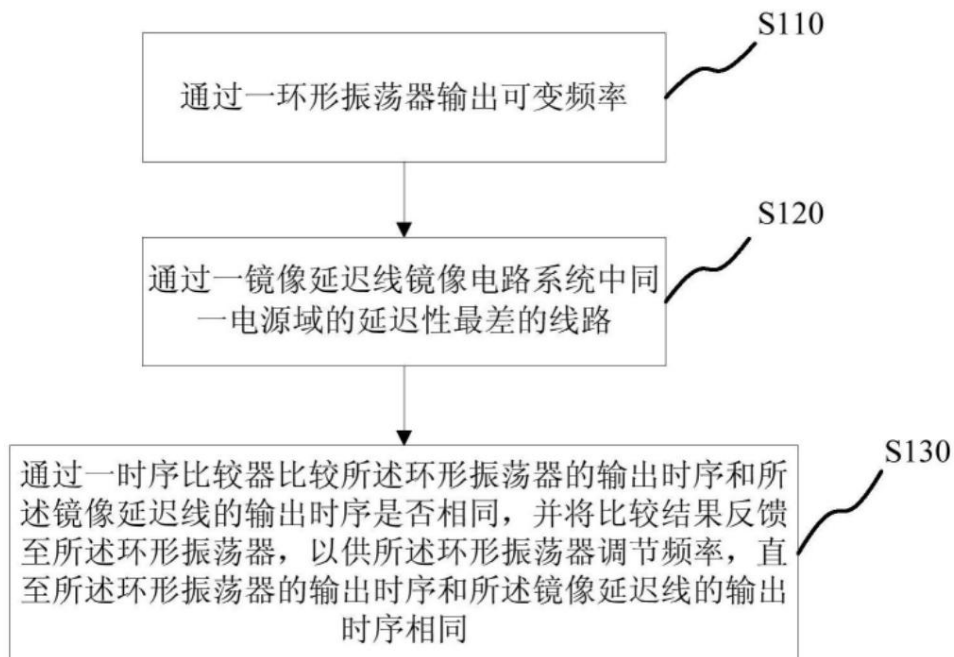


Figure 3

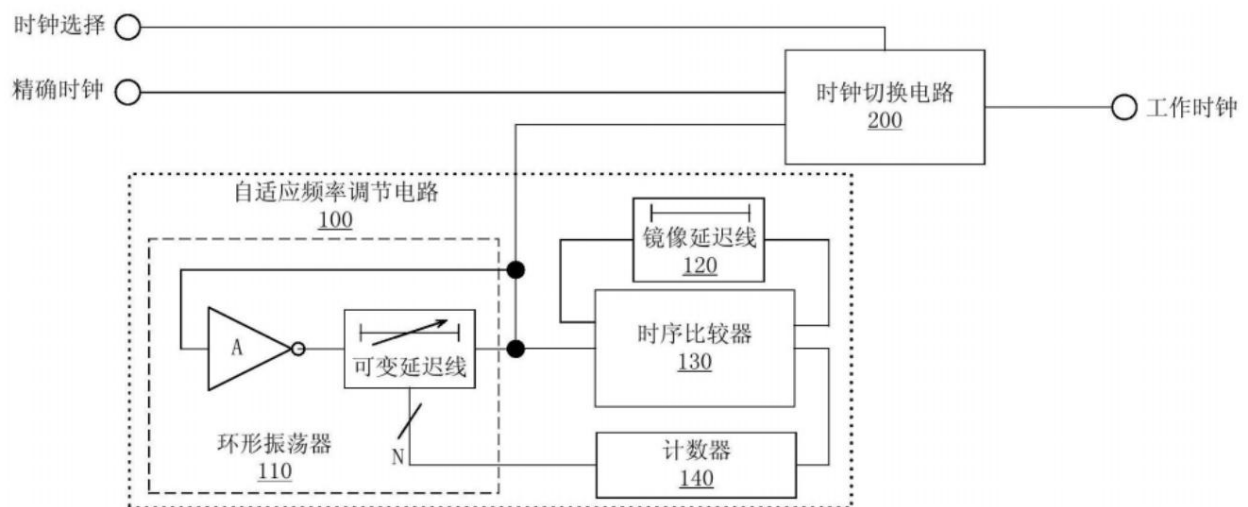


Figure 4